

NL17SZ126

Non-Inverting 3-State Buffer

The NL17SZ126 is a high performance single noninverting buffer operating from a 1.65 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with $V_{CC} = 3.0$ V
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3–State OE Input is Active HIGH
- Replacement for NC7SZ126
- Chip Complexity = 36 FETs
- Pb–Free Packages are Available

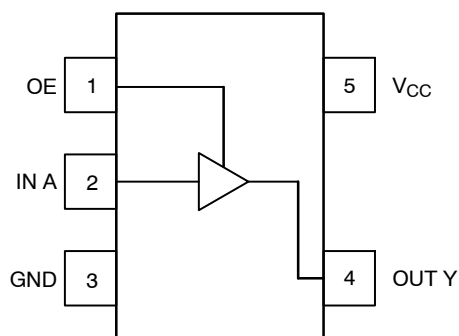


Figure 1. Pinout (Top View)

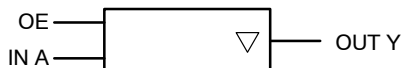


Figure 2. Logic Symbol



ON Semiconductor®

<http://onsemi.com>

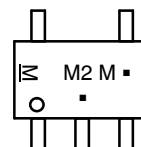


SC-88A (SOT-353)
DF SUFFIX
CASE 419A



SOT-553
XV5 SUFFIX
CASE 463B

MARKING DIAGRAM



M2 = Specific Device Code

M = Date Code

▪ = Pb–Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

PIN ASSIGNMENT	
1	OE
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

OE Input	A Input	Y Output
H	L	L
H	H	H
L	X	Z

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	- 0.5 to + 7.0	V
V _{IN}	DC Input Voltage	- 0.5 to + 7.0	V
V _{OUT}	DC Output Voltage	- 0.5 to + 7.0	V
I _{IK}	DC Input Diode Current	- 50	mA
I _{OK}	DC Output Diode Current	- 50	mA
I _{OUT}	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
T _{STG}	Storage Temperature Range	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+ 150	°C
θ _{JA}	Thermal Resistance	SC-70/SC-88A	350 °C/W
P _D	Power Dissipation in Still Air at 85°C	SC-70/SC-88A	150 mW
MSL	Moisture Sensitivity		Level 1
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	5.5	V
T _A	Operating Temperature Range	- 40	+125	°C
t _p , t _f	Input Rise and Fall Time	V _{CC} = 1.8 V ± 0.15 V V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 20 10 5.0	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

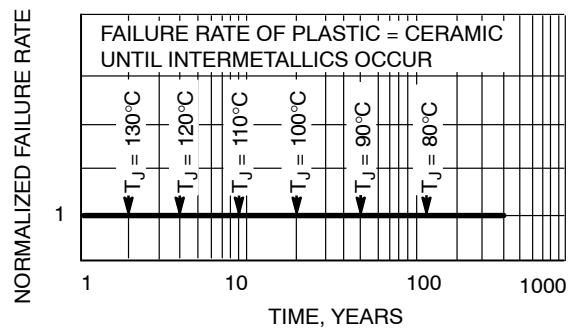


Figure 3. Failure Rate versus Time Junction Temperature

NL17SZ126

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit	Condition
			Min	Typ	Max	Min	Max		
V _{IH}	High-Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V	
V _{IL}	Low-Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IH}	1.65	1.55	1.65		1.55		V	I _{OH} = -100 μA
		1.8	1.7	1.8		1.7			
		2.3	2.2	2.3		2.2			
		3.0	2.9	3.0		2.9			
		4.5	4.4	4.5		4.4			
		1.65	1.29	1.52		1.29		V	I _{OH} = -4 mA
		2.3	1.9	2.15		1.9			I _{OH} = -8 mA
		3.0	2.4	2.80		2.4			I _{OH} = -16 mA
		3.0	2.3	2.68		2.3			I _{OH} = -24 mA
		4.5	3.8	4.20		3.8			I _{OH} = -32 mA
		1.65		0.0	0.1		0.1	V	I _{OL} = 100 μA
		1.8		0.0	0.1		0.1		
		2.3		0.0	0.1		0.1		
		3.0		0.0	0.1		0.1		
		4.5		0.0	0.1		0.1		
		1.65		0.08	0.24		0.24	V	I _{OL} = 4 mA
		2.3		0.10	0.30		0.30		I _{OL} = 8 mA
		3.0		0.15	0.40		0.40		I _{OL} = 16 mA
		3.0		0.22	0.55		0.55		I _{OL} = 24 mA
		4.5		0.22	0.55		0.55		I _{OL} = 32 mA
I _{IN}	Input Leakage Current	0 to 5.5			±1.0		±1.0	μA	0 V ≤ V _{IN} ≤ 5.5 V
I _{OZ}	3-State Output Leakage	1.65 to 5.5			±0.5		±5.0	μA	V _{IN} = V _{IH} or V _{IL} 0 V ≤ V _{OUT} ≤ 5.5 V
I _{OFF}	Power Off Leakage Current	0.0			1.0		10	μA	V _{IN} or V _{OUT} = 5.5 V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μA	V _{IN} = 5.5 V, GND

AC ELECTRICAL CHARACTERISTICS (t_r = t_f = 3.0 ns)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay AN to YN (Figures 4, and 5, Table 1)	R _L = 1 MΩ C _L = 15 pF	1.8 ± 0.15	2.0	9.5	12	2.0	12.5	ns
		R _L = 1 MΩ C _L = 15 pF	2.5 ± 0.2	1.0	3.4	7.5	1.0	8.0	
		R _L = 1 MΩ C _L = 15 pF R _L = 500 Ω C _L = 50 pF	3.3 ± 0.3	0.8		5.2	0.8	5.5	
		R _L = 1 MΩ C _L = 15 pF R _L = 500 Ω C _L = 50 pF	5.0 ± 0.5	0.5		4.5	0.5	4.8	
t _{PZH} t _{PZL}	Output Enable Time (Figures 6, 7 and 8, Table 1)	R _L = 250 Ω C _L = 50 pF	1.8 ± 0.15	2.0	9.0	10.5	2.0	12.5	ns
			2.5 ± 0.2	1.8		8.5	1.8	9.0	
			3.3 ± 0.3	1.2		6.2	1.2	6.5	
			5.0 ± 0.5	0.8		5.5	0.8	5.8	
t _{PHZ} t _{PLZ}	Output Disable Time (Figures 6, 7 and 8, Table 1)	R _L and R1 = 500 Ω C _L = 50 pF	2.5 ± 0.2	1.5		8.0	1.5	8.5	ns
			2.5 ± 0.2	1.5		8.0	1.5	8.5	
			3.3 ± 0.3	0.8		5.7	0.8	6.0	
			5.0 ± 0.5	0.3		4.7	0.3	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	9 11	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

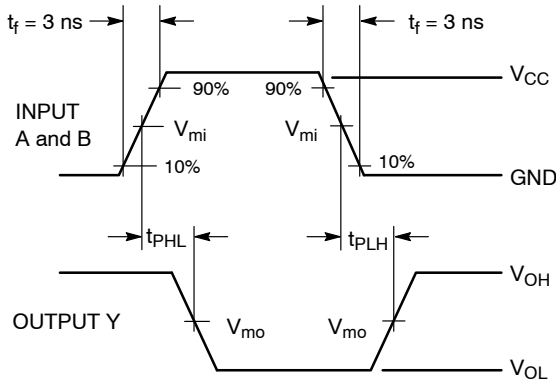
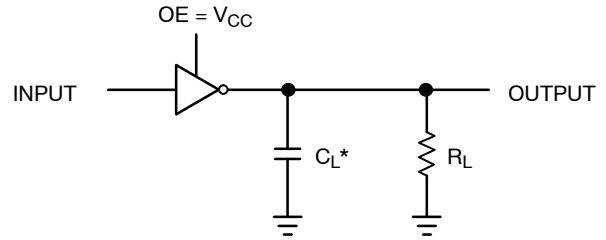
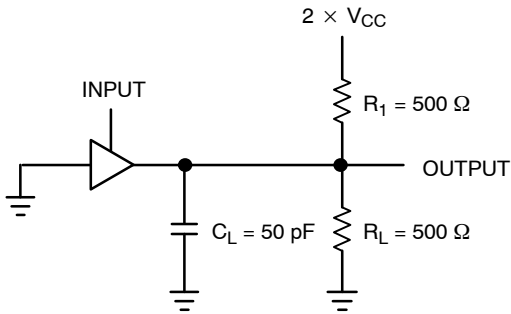


Figure 4. Switching Waveform



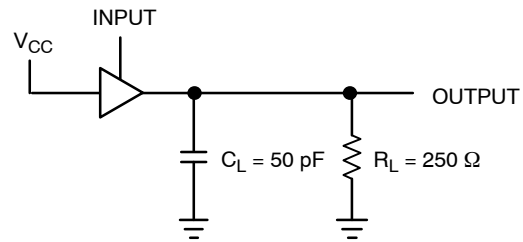
*Includes all probe and jig capacitance.
A 1-MHz square input wave is recommended for propagation delay tests.

Figure 5. T_{PLH} or T_{PLH}



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZL} or T_{PLZ}



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 7. T_{PZH} or T_{PHZ}

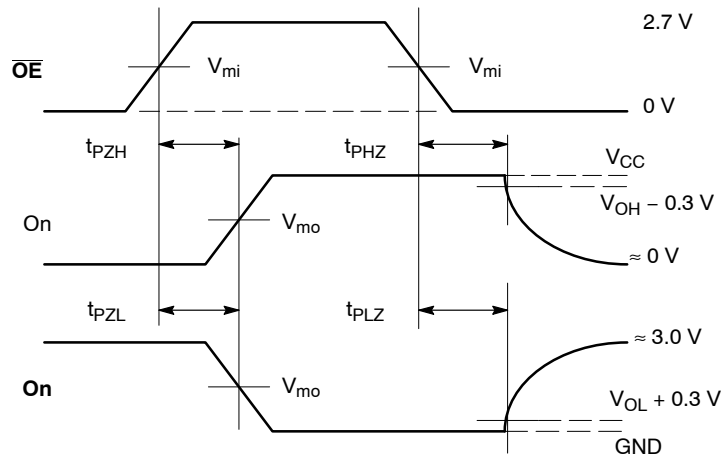


Figure 8. AC Output Enable and Disable Waveform

NL17SZ126

Table 1. Output Enable and Disable Times

$t_R = t_F = 2.5$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

Symbol	V_{CC}		
	$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$2.5\text{ V} \pm 0.2\text{ V}$
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

DEVICE ORDERING INFORMATION

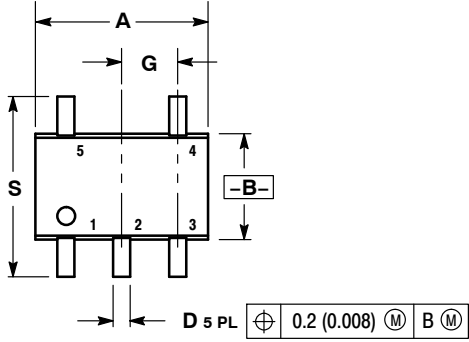
Device	Package Type	Shipping [†]
NL17SZ126DFT2	SC70-5/SC-88A/SOT-353	3000 / Tape & Reel
NL17SZ126DFT2G	SC70-5/SC-88A/SOT-353 (Pb-Free)	3000 / Tape & Reel
NL17SZ126XV5T2G	SOT-553 (Pb-Free)	4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NL17SZ126

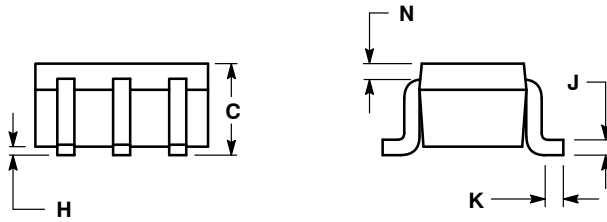
PACKAGE DIMENSIONS

SC-88A, SOT-353, SC-70
CASE 419A-02
ISSUE J

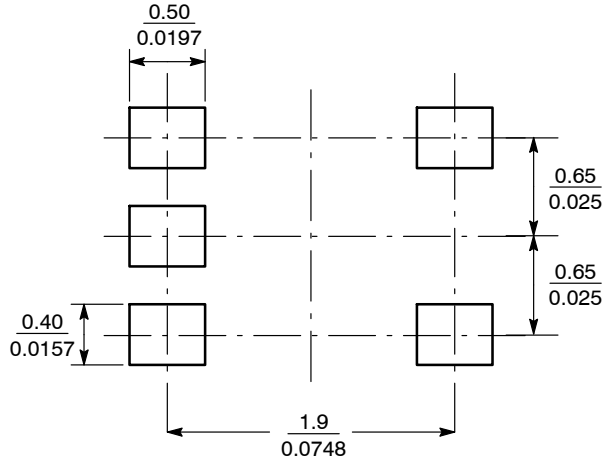


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



SOLDERING FOOTPRINT*

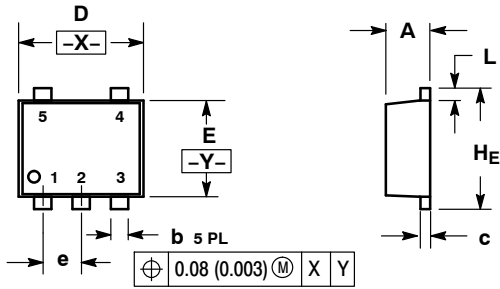


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ126

PACKAGE DIMENSIONS

SOT-553, 5 LEAD
CASE 463B-01
ISSUE B

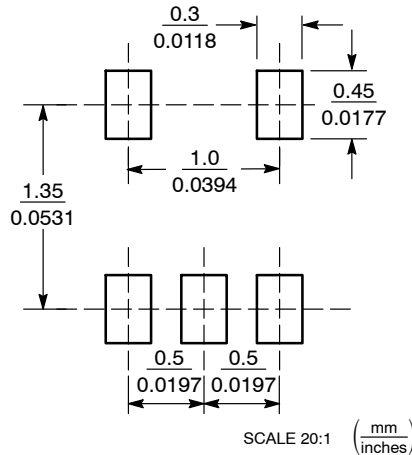


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative